EUROPEAN PATENT APPLICATION

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(54) Dynamic random-access memory.

(57) A dynamic random-access memory (DRAM) (11)
has a first refresh circuit (12) for producing memory
refreshes during power-up, and a second refresh
circuit (14) for producing memory refreshes during
power-down. The power-down refresh circuit (14) is
powered by a battery (15), and has a lower power
consumption than the power-up circuit. During transi-
tion from power-down to power-up, the frequency of
refreshing is doubled for a short period, so as to
build up a surplus of refreshes. This allows refresh-
ing the stop while the first or power-up refresh circuit
(12) is brought back into operation.

Fig. 1.

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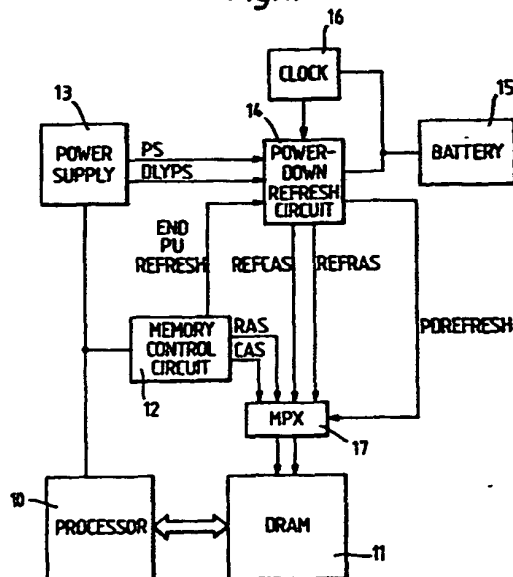
DYNAMIC RANDOM-ACCESS MEMORY.

Background to the Invention.

This invention relates to dynamic random-access memories (DRAMS).

In a DRAM, the contents of the memory gradually decay, and it is necessary to refresh the memory periodically in order to preserve its contents. This normally involves cycling through the memory and performing a read/write operation on each location of the memory in turn. Typically, each location must be refreshed every 4 milliseconds.

If the system in which the DRAM is used is switched off (powered down), then the contents of the DRAM may be lost. This can be avoided by providing some form of battery back-up for the memory, so that refreshing can continue even when the system is powered down.

It has been proposed to provide a dynamic random-access memory having a first refresh circuit for producing memory refresh cycles during a power-up condition, and a second refresh circuit for producing memory refresh cycles during a power-down condition and having a lower power requirement than the first refresh circuit. This enables the power requirements in the power-down conditions to be reduced, so as to avoid excessive drain on the battery.

When two refresh circuits are used in this way, it is necessary to switch between the two circuits when power is removed or restored. A problem arises in that, when power is restored, it is necessary to bring the power-up refresh circuit into operation quickly, to avoid loss of data. This may be difficult to achieve, since it may be necessary for a system processor to initialise the power-up refresh circuit before it can begin to operate.

According to the invention there is provided a dynamic random-access memory having a first refresh circuit for producing memory refresh cycles during a power-up condition, a second refresh circuit for producing memory refresh cycles during a power-down condition and having a lower power requirement than the first refresh circuit, and means operative during transition from the power-down condition to the power-up condition for temporarily increasing the frequency of the refresh cycles by the second refresh circuit, thereby providing a period in which no refresh cycles are required, to allow time for the first refresh circuit to become operative.

By increasing the frequency of the second refresh circuit during the transition, it is possible to build up a surplus of refreshes. This enables the memory to be left for a short period without any refreshes, while the first refresh circuit comes back

into operation.

In one embodiment of the invention, the frequency of the first refresh circuit is increased for a short period after the transition. This further ensures that each location of the memory is refreshed within the prescribed cycle time.

Brief description of the drawings.

One embodiment of the invention will now be described by way of example with reference to the accompanying drawings.

Figure 1 is a block diagram of a data processing system including a dynamic random-access memory (DRAM), with power-up and power-down refresh circuits.

Figures 2 and 3 are state diagrams describing the power-down refresh circuit.

Description of an embodiment of the invention.

Referring to Figure 1, the system comprises a processor 10, connected to a DRAM 11 so that the processor can read and write data in a conventional manner.

The DRAM 11 in this example holds 256K bytes, organised in 1024 rows and 256 columns. The DRAM has a memory control circuit 12, which may be of conventional form, for producing the normal row address strobe (RAS) and column address strobe (CAS) signals for the memory.

The system also includes a power supply unit 13, for supplying power to the processor, DRAM, and memory control circuit.

When the system is powered up (i.e. when the power supply 13 is operating) the memory control circuit 12 performs periodic refresh operations on the DRAM. Each refresh cycle consists of applying a CAS and then a RAS to the memory, i.e. reversing the normal order of RAS then CAS. This causes one selected column of the memory to be refreshed. The refresh cycle is performed for a different column every 15.625 microseconds, which means that the whole memory is refreshed every 4 milliseconds. This ensures that the memory contents are preserved.

The control circuit 12 is conveniently implemented as a plurality of integrated-circuit gate arrays, and hence has a relatively high power requirement.

When the system is powered down, the DRAM is refreshed by a power-down refresh circuit 14,

powered by a back-up battery 15. The power-down refresh circuit comprises a single CMOS chip, and hence consumes only a relatively small amount of power.

The power-down refresh circuit 14 receives a 512 KHz clock signal CLK from a clock circuit 16, which is also powered by the battery 15.

The power supply 13 produces two control signals PS and DLYPS, to indicate its current state. PS is true (high) when the power supply is operating normally. When the power supply is switched off, the signal PS goes false (low) before the supply voltage falls out of specification. When the power supply is switched on again, the signal PS goes true after the supply voltages are back within specification. DLYPS follows PS after a delay of greater than 2 milliseconds.

The control circuit 12 produces a control signal END PU REFRESH CYCLE to indicate the end of each power-up refresh cycle. This signal is fed to the power-down refresh circuit 14.

The system also includes a multiplexer 17, which normally selects the signals RAS and CAS from the memory control circuit 12 for application to the DRAM. When this mulitplexer is switched, as will be described below, it selects alternative signals REFRAS and REFCAS from the power-down refresh circuit 14.

The power-down refresh circuit 14 comprises two parts, referred to herein as the power-down/power-up control and the refresh control. Each of these parts is impemented in the form of a state machine, as defined by the state diagrams of Figure 2 and 3 respectively.

The power-down/power-up control (Figure 2) communicates with the refresh control (Figure 3) by means of the following signals:-
PD REFRESH. This enables the refresh control. As shown in Figure 1, this signal also controls the multiplexer 17, so that when PD REFRESH is true, the signals REFRAS and REFCAS are routed to the DRAM in place of the normal RAS and CAS.

DOUBLE REFRESH RATE. This causes the refresh control to double the refresh rate.

The refresh control communicates with the power-down/power-up control by means of the following signal:-
END PD REFRESH CYCLE. This indicates that the current power-down refresh cycle is complete.

In the state diagrams of Figures 2 and 3, each state is represented by a circle, and transition between states is represented by an arrow. Each arrow is labelled with one or more conditions which must be satisfied before the transition can take place, followed (in brackets) by output signals that are ffected by the transition.

For example, in Figure 2, the arrow from state A to state B is labelled with the conditions END PU

REFRESH CYCLE and /PS (where / denotes negation). Thus, if the state machine is in state A, then it will make the transition to state B at the first clock edge after these conditions are both satisfied. At the same time, th output PD REFRESH goes true. If, on the other hand, these two conditions are not both satisfied, then the state machine remains in state A and PD REFRESH remains false.

The operation of the two state machines will now be described.

In the power-down condition, PS is false. This causes the power-down/power-up control (Figure 2) to enter state B and to remain there, with DOUBLE REFRESH RATE false and PD REFRESH true. At the same time, the refresh control (Figure 3) cycles through the eight states K-S at successive clock beats, producing one REF CAS and one REF RAS in each cycle. Thus, in this condition, a refresh cycle is performed at every eighth clock beat, i.e. every 15.625 microseconds.

When the system is powered up, the signal PS goes true. At the next clock beat, the power-down/power-up control goes from state B to state C, and DOUBLE REFRESH RATE goes true. This signal causes the refresh control to loop back from state N to state K, so that it now cycles through the four states K-N, again producing a REFCAS and a REFRAS in each cycle. Thus, in this condition, a refresh cycle is produced every 7.812 microseconds, so that the refresh rate is doubled.

After 2 milliseconds, the signal DLYPS goes true. Then, at the first clock beat after END PD REFRESH CYCLE becomes true, the power-down/power-up control goes from state C to state A, and DOUBLE REFRESH RATE and PD RE-FRESH both become false. At the same time, the refresh control goes from state N to state K, and END PD REFRESH becomes false. PD REFRESH causes the processor 10 to come out of reset, and switches the mulitplexer 17 (Figure 1) so as to connect the normal control signals RAS and CAS to the memory.

The state machines remain in states A and K respectively, until the next power-down.

After the processor 10 has come out of reset the memory control circuit 12, under the control of software, doubles the refresh rate for a period of 2 milliseconds after which it reverts back to its normal rate. This ensures that those columns of memory refreshed at the beginning of the power-down refresh cycle are refreshed within 4 milliseconds of their last refresh.

In summary, it can be seen that, when the system is powered-up, the refresh rate of the power-down refresh control 14 is doubled for 2 milliseconds before the processor comes out of reset. This builds up a surplus of refresh cycles, such that the DRAM does not have to be refreshed

again for another 2 milliseconds. This allows time for the the processor to initialise the memory control circuit 12, so as to allow it to start performing refresh cycles again.

By also doubling th refresh rate after the processor has come out of reset it is ensured that every column of the memory is refreshed within 4 milliseconds of its last refresh.

Claims

1. A dynamic random-access memory having a first refresh circuit for producing memory refresh cycles during a power-up condition, a second refresh circuit for producing memory refresh cycles during a power-down condition and having a lower power requirement than the first refresh circuit, characterised in that during transition from the power-down condition to the power-up condition the frequency of the refresh cycles produced by the second refresh circuit (14) is temporarily increased, thereby providing a period in which no refresh cycles are required, to allow time for the first refresh circuit (12) to become operative.

2. A memory according to Claim 1 wherein after the transition from the power-down condition to the power-up condition the frequency of the refresh cycles produced by the first refresh circuit (12) is temporarily increased.

3. A memory according to Claim 1 and 2 wherein the frequency of the refresh cycles produced by the second refresh circuit (14) is increased for a predetermined period during the transition from the power-down condition to the power-up condition.

4. A memory according to Claim 1 or 2 wherein the frequency of the refresh cycles produced by the second refresh circuit (14) is doubled during the transition from the power-down condition to the power-up condition.

5. A memory according to any preceding claim wherein the second refresh circuit (14) includes a state machine which, during the power-down condition, cycles through a plurality of states (K-S), producing a refresh cycle in each cycle through the states, and which during transition from the power-down condition to the power-up condition, cycles through a smaller plurality of states(K-N), thereby producing refresh cycles with increased frequency.

6. A memory according to any preceding claim including a back-up battery (15) for supplying power to the second refresh circuit (14) during power-down.

7. A data processing system including a memory (11) according to any preceding claim, and a processor (10) connected to the memory.
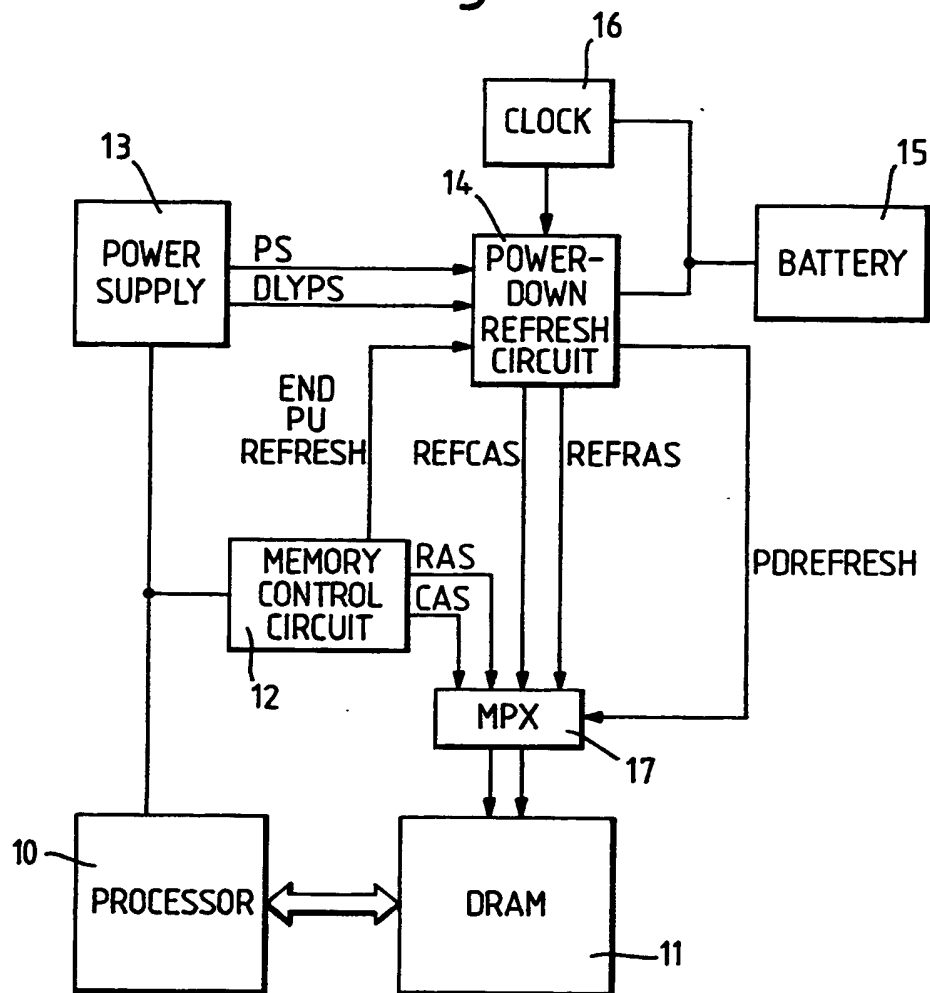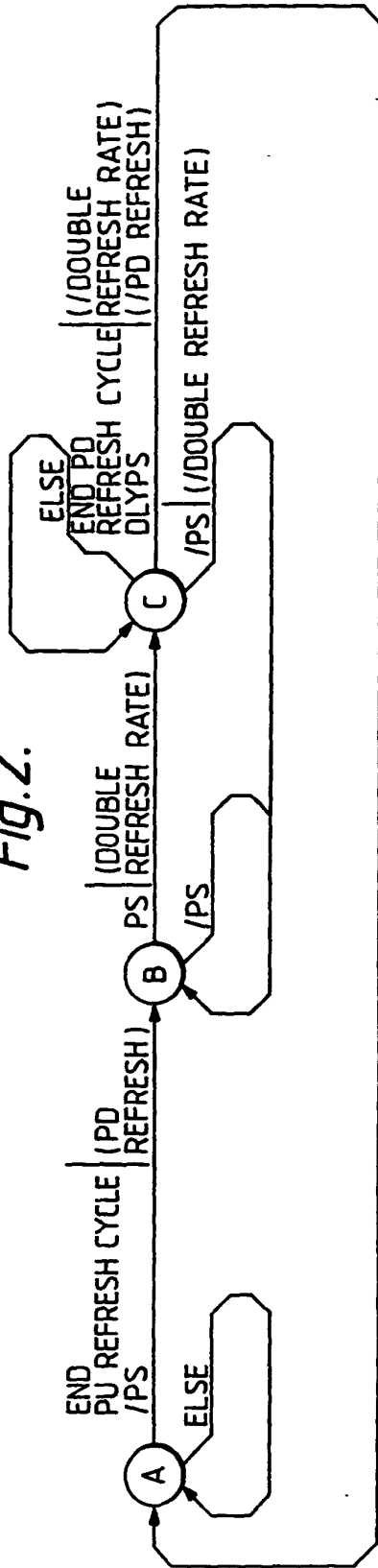
Fig.1.

Fig.2.

Fig.3.